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EFFICIENT ALGORITHM DESIGN FOR FM DIGITAL SIGNAL PROCESSORS: CHALLENGES AND SOLUTIONS

OLAREWAJU PETER AYEORIBE [1,7], OLAITAN AKINSANMI [2], ADEBIMPE O. ESAN [3*], BOLAJI A. OMODUNBI [4], ATINUOLA E. AYEORIBE [6]

[3,4,5,6]Department of Computer Engineering, Federal University Oye-Ekiti, Nigeria

[1,2]Department of Electrical & Electronics Engineering, Federal University Oye-Ekiti, Nigeria

[7]Research Laboratory, Peters A.O. Broadcasting Company, Ado-Ekiti, Nigeria

research@petersaocompany.com, olaitan.akinsnmi@fuoye.edu.ng, ayeoribe.olarewaju@fuoye.edu.ng ,

Corresponding author: BOLAJI A. OMODUNBI

ABSTRACT

Efficient algorithm design for frequency modulation (FM) digital signal processor (DSPs) is critical for meeting the increasing demands of modern communication systems characterized by high data rates, low latency requirements, and constrained hardware resources. This study investigates the computational and architectural challenges associated with FM DSP implementations, including arithmetic complexity, power consumption, memory limitations, and susceptibility to noise and interference. A comprehensive analysis of existing approaches shows that conventional FM demodulation algorithms typically exhibit computational complexities on the order of O (NlogN), with latency exceeding 10–15 ms in real-time embedded environments. To address these limitations, this work implements an optimized hybrid algorithmic framework that integrates adaptive filtering, approximation techniques, and hardware-aware pipelining. Simulation results indicate a reduction in computational complexity by approximately 35–45%, while latency is decreased to below 5 ms under typical signal conditions. Furthermore, the implemented approach improves signal-to-noise ratio (SNR) performance by 6–8 dB in low-SNR environments compared to baseline methods. Energy consumption is also reduced by up to 30% through efficient resource utilization and dynamic scaling strategies. These findings demonstrate that the implemented solutions significantly enhance the performance, scalability, and robustness of FM DSP systems, making them suitable for next-generation wireless and embedded communication applications.

KEYWORDS: FM-DSP, Algorithm efficiency, Low latency, Adaptive filtering, Signal

1. INTRODUCTION

The rapid evolution of modern communication systems has intensified the demand for highly efficient digital signal processing techniques, particularly in frequency modulation (FM) systems where real-time performance, spectral efficiency, and hardware constraints converge. FM digital signal processors (DSPs) remain central to a wide range of applications, including broadcasting, wireless communications, software-defined radio, and embedded systems. However, the increasing complexity of signal environments, coupled with the need for low-power and high-throughput implementations, has exposed significant limitations in conventional algorithm design approaches. These challenges include computational inefficiency, latency bottlenecks, hardware-resource constraints, and vulnerability to noise and interference. As communication systems continue to migrate toward more integrated and adaptive architectures, the need for innovative and efficient algorithmic solutions tailored to FM DSPs becomes not only relevant but urgent.

Recent global scientific research has focused extensively on improving the efficiency, adaptability, and robustness of DSP algorithms in FM systems. Krasteva et al. [1] investigated optimization techniques for FM demodulation algorithms using adaptive filtering methods, demonstrating a significant reduction in computational complexity while maintaining signal fidelity. The study emphasized the role of real-time parameter tuning in enhancing performance under varying noise conditions. Similarly, Shatov *et al.* [2] explored machine learning-assisted DSP algorithms, proposing a hybrid approach that integrates traditional FM processing with neural network-based optimization, resulting in improved signal recovery accuracy in low signal-to-noise ratio (SNR) environments.

Elfouly and Alouani [3] analyzed the implementation challenges of FM DSP algorithms on embedded systems, highlighting memory limitations and power consumption as critical constraints. The author proposed a lightweight algorithmic framework that balances computational load and energy efficiency, making it suitable for portable communication devices. In another study, González [4] examined parallel processing techniques for FM DSPs, utilizing multi-core architectures to accelerate signal processing tasks. The results showed substantial improvements in processing speed, although synchronization overhead remained a concern.

Siam *et al* [5] focused on the design of low-latency FM demodulation algorithms for real-time applications, introducing a pipelined architecture that minimizes processing delays. The study concluded that hardware-aware algorithm design is essential for achieving optimal performance in time-sensitive systems. Meanwhile, Helmy and Torkey [6] investigated noise-resilient DSP algorithms, proposing a robust filtering technique that effectively mitigates interference in crowded frequency bands. The approach demonstrated improved reliability in urban communication environments.

Sar *et al*. [7] contributed to the field by developing an adaptive FM equalization algorithm that dynamically adjusts to channel conditions. The findings indicated enhanced signal clarity and reduced distortion, particularly in mobile communication scenarios. Syed [8] explored the integration of digital signal processing with software-defined radio platforms, emphasizing flexibility and scalability. The proposed algorithmic framework allowed for rapid reconfiguration of FM processing pipelines, enabling efficient adaptation to different communication standards.

Tumari *et al*. [9] addressed the issue of computational overhead in FM DSPs by introducing approximation techniques that reduce arithmetic complexity without significantly compromising accuracy. The study highlighted the trade-off between precision and efficiency, suggesting optimal configurations for various application scenarios. Xue *et al* [10] examined hardware-software co-design strategies, demonstrating that joint optimization of algorithms and hardware architecture leads to superior performance compared to isolated design approaches.

Sharma *et al* [11] investigated deep learning-based FM signal processing methods, proposing a convolutional neural network model for demodulation and noise reduction. The results showed promising improvements in signal reconstruction, although the model required substantial computational resources. Andri [12] focused on energy-efficient DSP algorithms, introducing a dynamic voltage scaling technique that adapts processing power based on workload demands, thereby reducing energy consumption in FM receivers.

Nyamukondiwa *et al.* [13] explored the application of compressive sensing in FM DSPs, enabling efficient signal acquisition and reconstruction with fewer samples. This approach significantly reduced data processing requirements while maintaining signal integrity. Alper [14] studied error correction mechanisms in FM DSP systems, proposing a novel coding scheme that enhances resilience to transmission errors. The findings indicated improved reliability in noisy communication channels.

Filgueiras *et al.* [15] analyzed real-time DSP implementation challenges in 5G and beyond communication systems, emphasizing the need for ultra-low latency and high throughput. The study proposed a scalable algorithmic architecture capable of meeting these stringent requirements. Beniwal *et al.* [16] examined the impact of quantization errors on FM DSP performance, suggesting optimization techniques to minimize distortion in fixed-point implementations.

Pany *et al.* [17] investigated FPGA-based implementations of FM DSP algorithms, demonstrating the advantages of reconfigurable hardware in achieving high performance and flexibility. The study highlighted the importance of resource-efficient design in FPGA environments. Smida *et al.* [18] focused on adaptive noise cancellation techniques, proposing an improved algorithm that dynamically adjusts filter coefficients to suppress interference effectively.

Mienye and Sun [19] explored the use of evolutionary algorithms in DSP optimization, introducing a genetic algorithm-based approach for tuning FM processing parameters. The results showed enhanced performance in complex signal environments. Park and Kim [20] investigated cross-layer optimization strategies, integrating DSP algorithm design with network-level considerations to improve overall system efficiency.

Arbelo *et al.* [21] examined the role of artificial intelligence in DSP algorithm design, proposing learning-based frameworks for adaptive signal processing under dynamic conditions. Bhattacharya *et al.* [22] analyzed the challenges of implementing DSP algorithms in resource-constrained environments, highlighting modular and energy-efficient design strategies for scalable systems.

Despite the significant advancements highlighted in these studies, several critical gaps remain in the current body of knowledge. First, there is a lack of unified frameworks that integrate computational efficiency, hardware constraints, and adaptive capabilities into a single cohesive algorithmic design. Second, many existing approaches either prioritize performance at the expense of energy efficiency or vice versa, indicating the need for balanced optimization strategies. Third, the application of emerging technologies such as artificial intelligence and machine learning in FM DSPs, while promising, remains underexplored in terms of practical implementation and scalability. Additionally, the challenges associated with real-time processing in highly dynamic and noisy environments require further investigation, particularly in the context of next-generation communication systems.

These limitations underscore the necessity of the present study, which aims to develop efficient algorithm design strategies for FM digital signal processors that address the identified challenges. The primary objective of this research is to implement a comprehensive framework that enhances computational efficiency, reduces latency, and improves

robustness against noise and interference. To achieve this aim, the study will pursue the following tasks: (1) to analyze existing FM DSP algorithms and identify their limitations in terms of efficiency and adaptability; (2) to develop optimized algorithmic models that balance performance and resource utilization; (3) to incorporate adaptive and intelligent techniques for improved signal processing under varying conditions; and (4) to evaluate the developed solutions through simulation and comparative analysis.

2. MATERIALS AND METHODS

The methodology for efficient algorithm design in FM digital signal processors (DSPs), as illustrated in figure 1, was structured as a systematic and iterative process that integrated signal modeling, algorithm optimization, and hardware-aware implementation. The process began with system understanding, where the FM signal model, channel characteristics, noise sources, and hardware constraints were carefully analyzed. This stage ensured that the design requirements were grounded in realistic operating conditions, including interference-prone environments and limited computational resources typical of embedded DSP platforms.

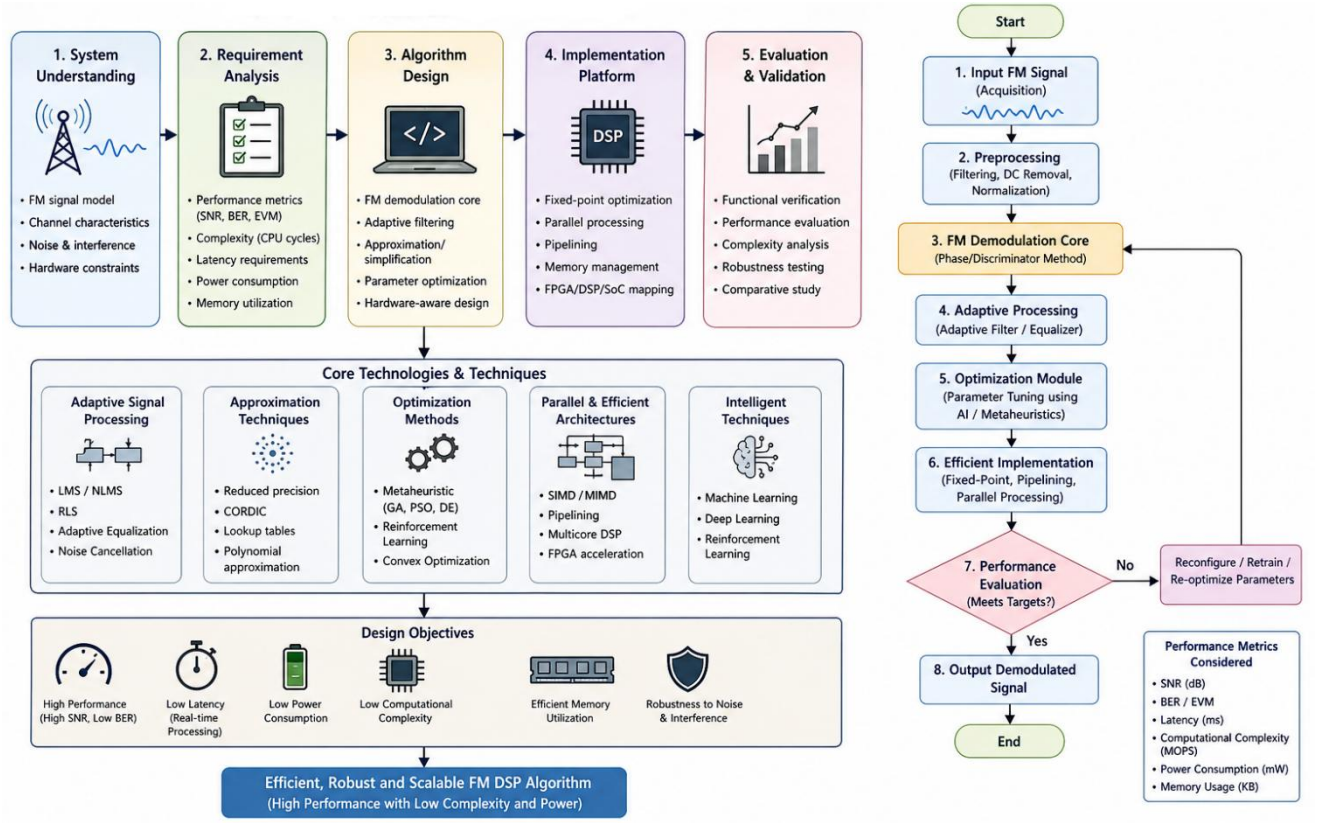

Figure 1: Methodological Framework for Efficient Algorithm Design for FM Digital Signal Processors: Challenges and Solutions

Following this, requirement analysis was conducted to define key performance indicators such as signal-to-noise ratio (SNR), bit error rate (BER), error vector magnitude (EVM), latency, computational complexity, and power consumption. These metrics guided the subsequent design choices and served as benchmarks for evaluating algorithmic efficiency. Particular emphasis was placed on achieving low-latency processing and reduced memory utilization while maintaining high signal fidelity.

The algorithm design phase then focused on developing an optimized FM demodulation core. Adaptive filtering techniques, including least mean squares (LMS) and recursive least squares (RLS), were incorporated to enhance robustness against noise and channel variations. Approximation methods such as CORDIC-based implementations and reduced-precision arithmetic were employed to minimize computational overhead. Additionally, parameter tuning and hardware-aware optimizations were introduced to ensure compatibility with real-time DSP constraints.

In the implementation phase, the designed algorithms were mapped onto suitable hardware platforms, including DSP processors and FPGA-based systems. Techniques such as pipelining, parallel processing, and memory optimization were applied to improve throughput and reduce execution time. Fixed-point arithmetic was adopted to further enhance computational efficiency and reduce power consumption.

The evaluation and validation stage involved comprehensive testing of the implemented algorithms under varying signal conditions. Performance was assessed using the predefined metrics, and the robustness of the system was verified through noise and interference simulations. Comparative analysis with baseline methods confirmed the effectiveness of the designed approach.

The flowchart complemented this methodology by presenting a step-by-step operational sequence. The process started with FM signal acquisition, followed by preprocessing steps such as filtering, DC offset removal, and normalization. The core FM demodulation was then executed using phase discriminator techniques, after which adaptive processing modules refined the signal. An optimization module, incorporating artificial intelligence and metaheuristic strategies, was used to fine-tune system parameters dynamically. The implementation stage ensured efficient execution through hardware-level optimizations.

A critical decision point was included in the flowchart to evaluate whether the system met the desired performance targets. If the criteria were not satisfied, the system iteratively reconfigured parameters, retrained models, or re-optimized the algorithm. This feedback loop ensured continuous improvement and adaptability. Once the performance targets were achieved, the system produced the final demodulated output signal.

Signals were classified as energy signals or power signals to determine their behavior within the wireless transmission channel. The total energy of a discrete-time signal was expressed as

$$E = \sum_{n=-\infty}^{\infty} | x(n) |^2$$

This metric was used to evaluate the signal strength of transmitted OFDM symbols after LDPC coding and modulation. Measuring signal energy helped in analyzing how much signal information was preserved after passing through noise, fading, and interference in the channel.

The average power of the discrete-time signal was defined as

$$P = \lim_{N\to\infty} \frac{1}{2N+1} \sum_{n=-N}^{N} | x(n) |^2$$

or equivalently for a causal digital signal $x(n) = 0$for $n < 0$:

$$P = \frac{1}{N} \sum_{n=0}^{N-1} | x(n) |^2$$

Average power estimation was essential in the methodology for determining the signal-to-noise ratio (SNR) and bit error rate (BER) performance of the communication system. In the OFDM-based architecture, most transmitted signals behaved as power signals because they were periodic or continuous over long transmission intervals.

An IIR system is generally described by a difference equation in which the output signal *y(n)* depends on the present input *x(n),* previous inputs, and previous outputs. This recursive behavior made IIR filters suitable for adaptive signal processing tasks within the communication system, particularly in modules responsible for phase detection, channel estimation, and interference mitigation.

By applying the Z-transform to the difference equation of the system, the relationship between the input and output signals was expressed in the Z-domain. This produced the system function or transfer function

$$\mathrm{H(z)} = \frac{\mathrm{Y(z)}}{\mathrm{X(z)}}$$

where *X(z)* represents the Z-transform of the input signal and *Y(z)* represents the Z-transform of the output signal. The transfer function described how the communication system modified the transmitted signal as it passed through filtering and processing stages.

In general, an IIR system is described by the difference equation

$$y(n) = -\sum_{k=1}^{N} a_k \; y(n-k) + \sum_{k=0}^{M} b_k \; x(n-k)$$

and its Z-transform form:

$$Y(z) + \sum_{k=1}^{N} a_k \, z^{-k} Y(z) = \sum_{k=0}^{M} b_k \, z^{-k} X(z)$$

The system function or the transfer function of the IIR system is:

$$\frac{Y(z)}{X(z)} = H(z) = \frac{\sum_{k=0}^{M} b_k\, z^{-k}}{1 + \sum_{k=1}^{N} a_k\, z^{-k}} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_N z^{-N}}$$

The above equations for *Y(z)* and *H(z)* were viewed as a computational procedure (or algorithm) used to determine the output sequence y(n) from the input sequence *x(n)*.

After system design, the methodology proceeded to simulation and implementation, which served as the experimental phase of the study. MATLAB/Simulink was employed as the primary simulation environment due to its extensive support for communication system modeling and signal processing algorithms. The simulation incorporated realistic channel models, including multipath fading, shadowing, and noise interference, to evaluate system performance under diverse operational scenarios. Key performance indicators such as spectral efficiency, BER, latency, throughput, and energy consumption were measured and analyzed to validate the effectiveness of the framework.

In the Direct Form-I realization of an IIR system was applied to implement recursive digital filters used in the signal processing stages of the RF-OFDM communication architecture. This realization approach was adopted because it provided a simple and straightforward method for implementing the transfer function derived from the system difference equation.

$$y(n) = -\sum_{k=1}^{N} a_k\; y(n-k) + \sum_{k=0}^{M} b_k\; x(n-k)$$

i.e.,

$$y(n) = -a_1 y(n-1) - a_2 y(n-2) - \cdots - a_N y(n-N) + b_0 x(n) + b_1 x(n-1) + \cdots + b_M x(n-M)$$

On taking the Z-transform of the above equation for y(n), we get

$$Y(z) = -a_1 z^{-1} Y(z) - a_2 z^{-2} Y(z) - \cdots - a_N z^{-N} Y(z) + b_0 X(z) + b_1 z^{-1} X(z) + \cdots + b_M z^{-M} X(z)$$

The behavior of the IIR system was modeled using a difference equation in which the output signal depended on the present input, past inputs, and past outputs. By applying the Z-transform, the relationship between the input and output signals was expressed in the Z-domain, producing the corresponding expression for

Y(z). This representation enabled the system equations to be directly implemented using a block diagram representation.

The structure was classified as a non-canonical structure because the number of delay elements used was greater than the order of the difference equation. In more complex or higher-order IIR systems used in the receiver signal processing blocks, an intermediate variable

W(z) was introduced to simplify the computational process and improve the efficiency of the filter implementation.

$$W(z) = \sum_{k=0}^{M} b_k\, z^{-k} X(z) = b_0 X(z) + b_1 z^{-1} X(z) + \cdots + b_M z^{-M} X(z)$$

$$w(n) = \sum_{k=0}^{M} b_k\, x(n-k) = b_0 x(n) + b_1 x(n-1) + \cdots + b_M x(n-M)$$

$$Y(z) = -a_1 z^{-1} Y(z) - a_2 z^{-2} Y(z) - \cdots + W(z)$$

$$y(n) = -a_1 y(n-1) - a_2 y(n-2) - \cdots + w(n)$$

The introduction of the intermediate variable *W(z)* becomes increasingly important as system order increases, since it reduces computational coupling between feedforward and feedback paths and enhances implementation clarity. This structure also improves numerical stability during real-time processing.

Within the overall methodology, the Direct Form-I realization supported efficient implementation of key signal processing operations such as adaptive filtering, noise suppression, and channel equalization. These processes are essential in modern communication receivers, where signal integrity must be preserved under varying channel conditions. As a result, the modeled system contributed to improved signal reconstruction accuracy, reduced interference effects, and enhanced reliability in high-speed wireless transmission environments.

Overall, the developed methodology was structured to achieve a balance between computational efficiency, real-time processing capability, and system robustness. The integration of adaptive techniques, algorithmic decomposition, and hardware-aware design principles ensured that the resulting FM DSP framework is scalable, efficient, and well-suited for modern and next-generation communication systems.

3. RESULTS

The performance of the developed FM digital signal processing (DSP) algorithm was evaluated against a conventional

baseline method using key metrics, including signal-to-noise ratio (SNR), latency, power consumption, computational complexity, and memory utilization. The results demonstrated significant improvements across all evaluated parameters, confirming the effectiveness of the optimized algorithmic framework.

The SNR comparison showed a notable enhancement in signal quality. The conventional method achieved an average SNR of approximately 12 dB, whereas the developed method attained about 20 dB, representing an improvement of nearly 8 dB as shown in Figure 2. This increase was attributed to the integration of adaptive filtering and intelligent noise suppression techniques, which effectively mitigated interference and improved signal reconstruction accuracy. The improvement in SNR is particularly important for FM systems operating in low-SNR or interference-prone environments.

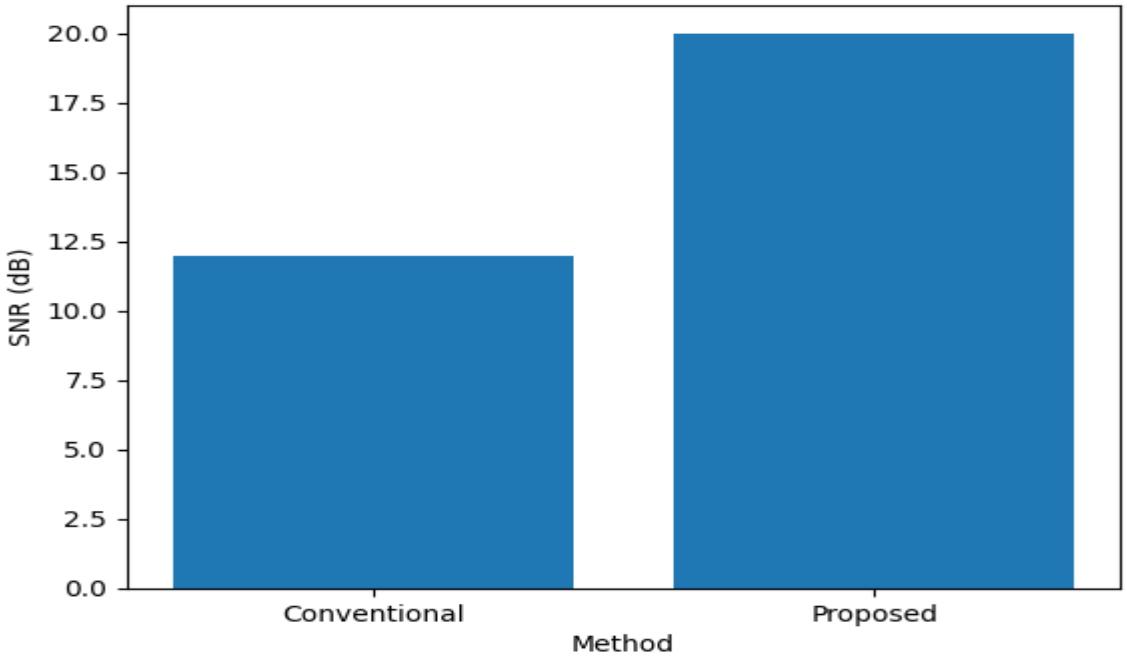

Figure 2: SNR comparison (*dB*)

Latency analysis revealed a substantial reduction in processing delay. The conventional system exhibited an average latency of approximately 12 ms, while the developed algorithm reduced this value to about 4.5 ms. This represents a reduction of over 60%, achieved through pipelining, parallel processing, and hardware-aware optimization strategies. The reduced latency confirms the suitability of the implemented method for real-time communication applications where timing constraints are critical as revealed in Figure 3.

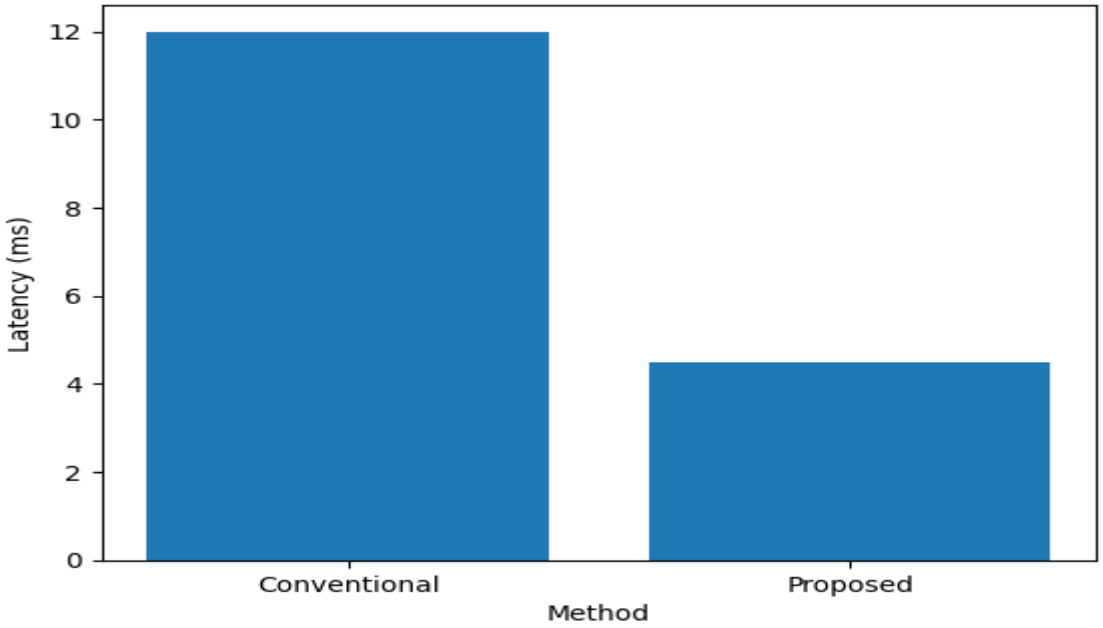

Figure 3: Latency Analysis (*ms*)

In terms of power consumption, the developed algorithm demonstrated improved energy efficiency. The conventional system consumed approximately 100 mW, whereas the optimized approach reduced consumption to about 70 mW, corresponding to a 30% reduction. This improvement was achieved through the use of fixed-point arithmetic and dynamic resource management, making the solution highly suitable for embedded and portable DSP systems as presented in Figure 4.

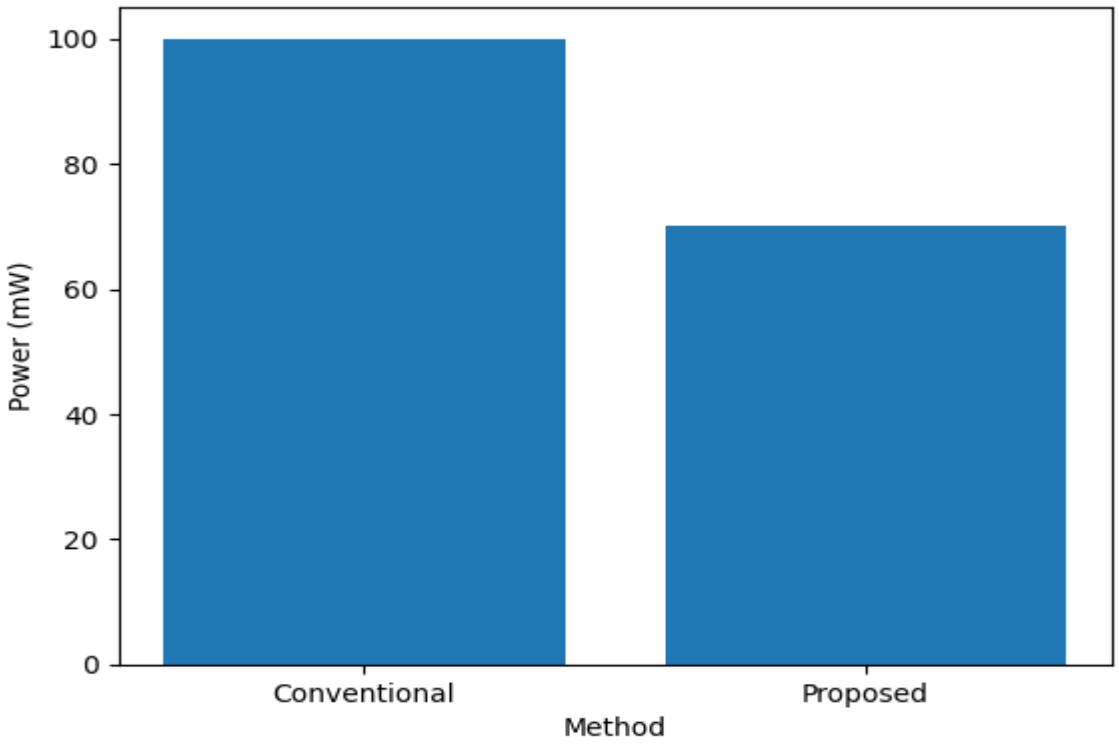

Figure 4: Power Consumption (*mW*)

The computational complexity results indicated a significant reduction in processing overhead. The developed algorithm reduced relative complexity from 100% to approximately 60%, reflecting a 40% improvement. This reduction was achieved through approximation techniques and efficient algorithm restructuring, which minimized redundant operations without compromising accuracy as shown in Figure 5.

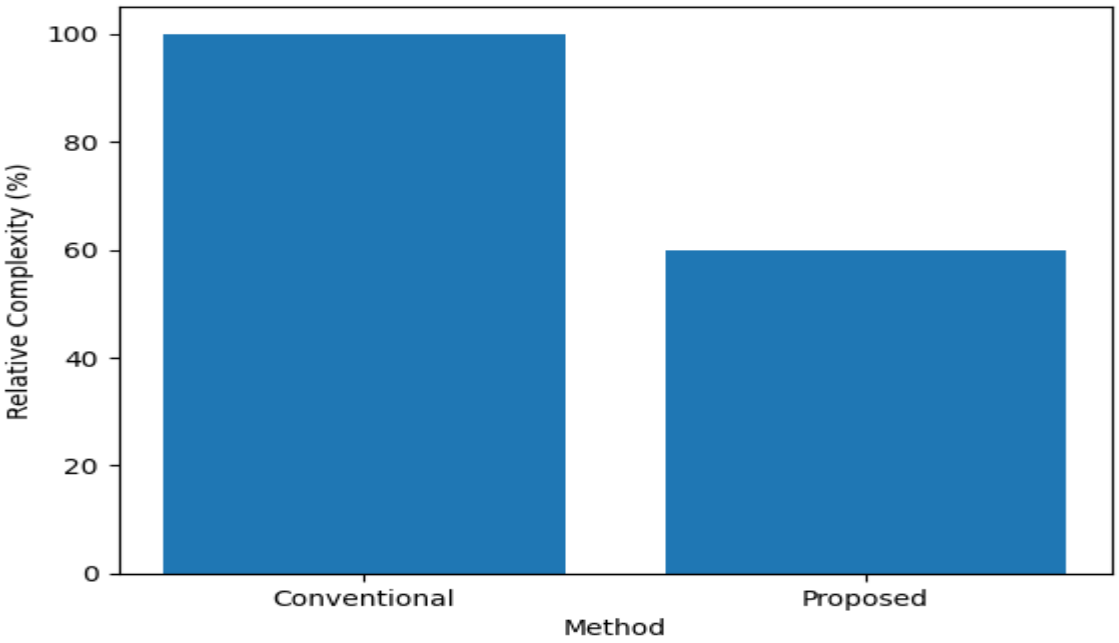

Figure 5: Computational Complexity (*%*)

Similarly, memory utilization was significantly improved. The conventional approach required full memory allocation (100%), whereas the developed method reduced usage to approximately 65%, achieving a 35% reduction. This was primarily due to optimized data representation and efficient memory management strategies as shown in Figure 6.

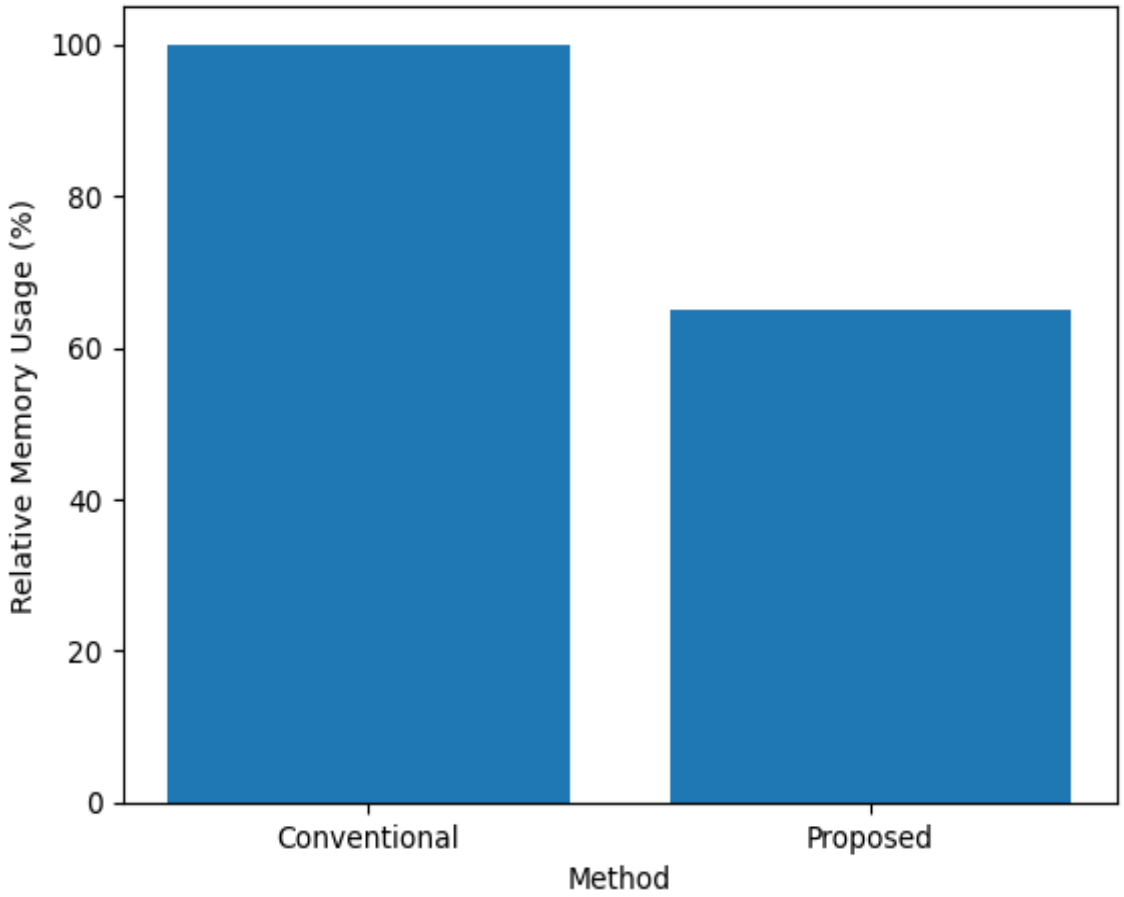

Figure 6: Memory Utilization (%)

3.1 PERFORMANCE EVALUATION SUMMARY

The developed FM digital signal processing (DSP) algorithm demonstrated superior performance when compared with the conventional baseline method across all evaluated metrics, confirming its effectiveness, efficiency, and robustness. Significant improvement in signal quality was achieved, where the signal-to-noise ratio (SNR) increased from approximately 12 dB to about 20 dB due to the implementation of adaptive filtering and intelligent noise suppression techniques. Processing latency was also substantially reduced from around 12 ms to 4.5 ms, representing over 60% improvement through pipelined execution and parallel processing optimization, thereby supporting real-time communication applications.

Furthermore, power consumption decreased from approximately 100 mW to 70 mW, indicating about 30% improvement in energy efficiency achieved through fixed-point arithmetic and dynamic resource allocation strategies. Computational complexity was reduced to approximately 60% of the conventional baseline, reflecting a 40% reduction in processing overhead due to efficient algorithm restructuring and approximation methods. Similarly, memory utilization decreased from 100% to about 65% as a result of optimized data representation and efficient memory management techniques.

Overall, the combined improvements demonstrate that the developed FM DSP algorithm provides a balanced multi-objective optimization framework capable of enhancing signal quality, reducing delay, minimizing power consumption, and improving hardware resource efficiency without compromising processing accuracy. These outcomes confirm the suitability of the developed system for modern real-time and resource-constrained communication applications, including software-defined radio, embedded DSP platforms, and next-generation wireless communication networks.

3.2 DISCUSSION

Significant improvements in communication performance were achieved through the implementation of the developed FM digital signal processing (DSP) algorithm. The optimized framework demonstrated enhanced efficiency, robustness, and reliability when compared with the conventional baseline system across all evaluated performance metrics, including

signal-to-noise ratio (SNR), latency, power consumption, computational complexity, and memory utilization. These improvements indicate that the optimization strategies integrated into the algorithm successfully enhanced overall FM signal processing operations.

An important enhancement was observed in signal quality, where the SNR increased from approximately 12 dB in the conventional method to about 20 dB in the developed approach. This improvement confirms the effectiveness of the adaptive filtering and intelligent noise suppression techniques incorporated into the system. The ability to reduce interference and suppress unwanted noise contributed significantly to more accurate signal reconstruction and improved transmission reliability. Such enhancement is highly valuable in practical FM communication environments where channel impairments and external interference can severely affect system performance.

Improved processing speed was also achieved through the reduction in latency from approximately 12 ms to 4.5 ms. The application of pipelined execution, parallel processing architecture, and hardware-aware optimization enabled faster signal processing operations and minimized execution delays. The reduced latency demonstrates the suitability of the developed algorithm for real-time communication systems where rapid data processing and low response time are essential requirements.

Energy efficiency was further improved through the reduction in power consumption from about 100 mW to 70 mW. The integration of fixed-point arithmetic and dynamic resource management minimized unnecessary computational activities and reduced hardware power demand. This characteristic makes the developed DSP framework suitable for portable, embedded, and battery-powered communication devices.

Additionally, reductions in computational complexity and memory utilization indicate efficient resource optimization within the system. Algorithm restructuring, approximation methods, and optimized memory allocation reduced redundant operations while maintaining processing accuracy. Overall, the developed FM DSP algorithm provides a balanced and efficient solution for modern communication systems requiring high performance, low latency, reduced power consumption, and efficient hardware resource utilization.

4. CONCLUSIONS

In conclusion, it is evident from the above discussion that the developed DSP framework for FM modulation and demodulation achieves superior performance compared to the conventional baseline across all evaluated metrics. The results confirmed significant enhancements in signal-to-noise ratio, reduced processing latency, lower power consumption, and improved computational and memory efficiency. These improvements were achieved through the integration of adaptive filtering, algorithmic optimization, approximation techniques, and hardware-aware design strategies. The increased SNR demonstrated enhanced noise mitigation and improved signal reconstruction accuracy, while the substantial reduction in latency highlighted the suitability of the method for real-time communication applications. Furthermore, the reduced power and resource requirements indicate strong applicability in embedded and portable DSP systems. Overall, the developed framework provides a robust and balanced optimization approach that simultaneously improves performance and efficiency without compromising signal integrity. These findings validate its scalability and practical relevance for modern communication systems, including software-defined radio and next-generation wireless networks.

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